

PRINTED WIRING BOARD AND ITS MANUFACTURE

Publication number: JP2000244101 (A)

Publication date: 2000-09-08

Inventor(s): HIROSE NAOHIRO

Applicant(s): IBIDEN CO LTD

Classification:

- international: H05K3/34; H05K1/18; H05K3/22; H05K3/34; H05K1/18; H05K3/22; (IPC1-7): H05K3/22; H05K1/18; H05K3/34

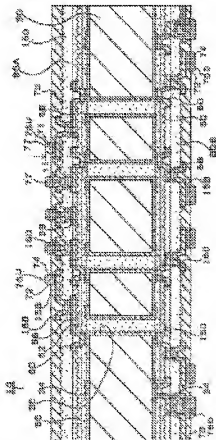
- **European:**

Application number: JP19990038394 19990217

Priority number(s): JP19990038394 19990217

Abstract of JP 2000244101 (A)

PROBLEM TO BE SOLVED: To establish a reliable junction between an IC chip and a conductor circuit by forming a solder resist layer having a plurality of openings on a substrate and forming a solder bump in each opening and then flattening the tops of part of the solder bumps. **SOLUTION:** A conductor circuit 34 is formed on both sides of a core substrate 30 of a multilayer printed wiring board 10 and built-up interconnection layers 80A, 80B are formed on the conductor circuits 34. The built-up interconnection layer 80A comprises a via hole 60 and an interlayer resin insulating layer 50 formed with a conductor circuit, and the built-up interconnection layer 80B comprises a via hole 160 and an interlayer resin insulating layer 150 formed with a conductor circuit 158.; Then, a solder resist layer 70 is formed on the via hole 160 and on the conductor circuit 158, solder bumps 76U, 76D are formed through a plurality of openings 71 formed in the solder resist layers 70, and the tops of the solder bumps 76U are formed into flat tops 77.



Data supplied from the **esp@cenet** database — Worldwide